



CURRICULUM VITAE ABREVIADO (CVA)

Part A. PERSONAL INFORMATION *

First name	Almudena		
Family name	Lindoso		
Gender (*)	Female	Birth date (dd/mm/yyyy)	
Social Security, Passport, ID number			
e-mail	alindoso@inguc3m.es	URL Web	https://researchportal.uc3m.es/display/inv35272
Open Researcher and Contributor ID (ORCID) (*)	0000-0001-5870-6493		

(*) Mandatory

A.1. Current position

Position	Associate professor		
Initial date	28-09-2020		
Institution	University Carlos III de Madrid (UC3M)		
Department/Center	Electronic Technology	EPS	
Country	Spain	Teleph. number	
Key words	Fault tolerance, hardware acceleration, microprocessors, FPGA, radiation effects, COTS, reliability		

A.2. Previous positions (research activity interruptions, indicate total months)

Period	Position/Institution/Country/Interruption cause
2015-2020	Visiting teacher/UC3M/Spain
2004-2015	Assistant teacher/UC3M/Spain Interruption of 8 months: maternities (2011) and (2013)
2003-2004	PhD formation scholarship

A.3. Education

PhD, Licensed, Graduate	University/Country	Year
PhD	University Carlos III de Madrid	2009
Telecommunication Engineer	University Politécnica de Madrid	2001

Part B. CV SUMMARY

Since 2003 I have been professor in the Electronic Technology Department of the UC3M, and Associate Professor since 2020. I have 3 sexenios and 4 quinquenios and I have been awarded with competitive UC3M complements for my outstanding activity in: teaching (2024, 2022) research (2018,2016) and publications (2024,2022,2018,2016,2014).

My research activity involves 2 main fields: image processing with high performance hardware architectures (hardware acceleration) and fault tolerant circuits. The first one is directly linked with my PhD, I have worked on several research projects in this field such as: development of a touchless fingerprint sensor (TBS) and PERIGEO project that adapted UAV technology for Space (Deimos & GMV). During my PhD, I did a 3-month PhD stay at University of Bologna (Italy).

My main research area is located in the Fault Tolerance field, in which I lead a research line of COTS (Commercial Off The Shelf) fault tolerant high-end complex digital systems. I have directed 4 PhDs in this topic, defended in 2017 (4 JCR), 2022 (7 JCR), 2023 (8 JCR) and 2024 (8 JCR). The PhD defended in 2022 was an Industrial PhD with CAM funding done in Arquimea aerospace company. This PhD received the Outstanding thesis award by UC3M and the research obtained funding from ESA through a competitive call (COTS usage in Space) in OSIP platform.

I collaborate regularly with international entities: UFRGS (Brazil), U. Montpellier (France), Politecnico di Torino (Italy), CERN (Switzerland) and Spanish ones: University of Alicante, U. Jaume I and CNA (Centro Nacional de Aceleradores).

I have participated in 21 competitive research projects (2 European projects and 2 competitive ESA calls) and 15 contracts, being IP in 4 of them. My last projects are quite relevant and linked to my research topic:

- NeCOT, competitive Spanish Gov. project to study and adapt commercial complex system on chip to their usage in Space.
- 2 ESA competitive projects in collaboration with the company Arquimea, both are aimed for increasing the reliability of circuits in space missions: one for formal verification (2018-2019) and another one linked with the research results of a recent industrial PhD (2021-2023).
- The EU project RADNEXT which joins all the European radiation facilities, being UC3M one of the few European research academic teams and the only Spanish University.
- RENASER4, (competitive Spanish Gov. 2019-2023), in which I have studied the heterogenous systems for space applications, proposing hardening techniques for multicore microprocessors, reusing microprocessor trace interface for hardware observation purposes, and proposing hardware techniques to improve reliability of FPGAs and GPUs.
- MadridFlightonChip, (CAM/EU) technological HUB in space, led by Sener Aeroespacial, in which I led the task of new techniques for COTS usage in Space missions.

I also collaborate with the Sener aeroespacial-UC3M chair (st3llar), one of my TFM students was awarded with the 2nd prize of the chair (2021) with a work about reliable high-end multicore microprocessors.

I have coauthored 47 JCR publications (plus two works under review), being highly relevant 39 of them (Q1 & Q2). 27 of my publications are from the last 5 years. I have coauthored more than 59 international conferences communications and 6 book chapters. The impact of my research according to google scholar is 1256 citations (h=21) and according to Scopus is: 727 citations (h=16).

I am a recognized member of the international research community of radiation effects in electronics: I have been member of program committee of the conference IEEE DFT since 2023, member of the awards committee of RADECS 2024, session chair and part of the technical committee of RADECS 2025 (Radiation effects in complex devices and Systems) and NSREC 2026 (Radiation hardness assurance) and invited speaker in SERESSA 2024. I am IEEE senior member and regular reviewer of the most important journals and conferences of my research area (since 2018, 50 reviews listed by ORCID). Since December of 2025 I am Deputy Director of the UC3M degree “Ingeniería Electrónica, Industrial y Automática” and from 2021 to 2024 I was TFG coordinator of 3 UC3M degrees. Since 2024 I have been elected faculty representative in EPS-UC3M Junta de Escuela and I am also member of the academic commission of the UC3M degrees of Robotics Engineering (since 2024) and Telematics Engineering (2020-2024). I was supervisor in the program “Research lab” of the International School of UC3M (summer 2024), tutoring research activities of international students from USA.

Part C. RELEVANT MERITS

C.1. Publications

1. P. M. Aviles, L.A: García-Astudillo, L. Entrena, M. García-Valderas, P. Martin-Holgado, Y. Morilla, A. Lindoso, Hardening Architectures for Multiprocessor System-on-Chip, in IEEE Transactions on Nuclear Science, vol. 71, no. 8, pp. 1887-1895, Aug. 2024. (7/7) AC. A. Lindoso.
2. P. M. Aviles, J. A. Belloch, L. Entrena and A. Lindoso, Supervised Triple Macrosynchronized Lockstep (STMLS) Architecture for Multicore Processors, in IEEE Access, vol. 11, pp. 128706-128723, 2023. (4/4) AC. A. Lindoso.
3. L. A. García-Astudillo, L. Entrena, A. Lindoso and H. Martín, Reduced Resolution Redundancy: A Novel Approximate Error Mitigation Technique, in IEEE Access, vol. 10, pp. 20643-20651, 2022. (3/4) AC: L.A. Garcia-Astudillo.
4. P. M. Aviles, A. Lindoso, J. A. Belloch, M. Garcia-Valderas, Y. Morilla, L. Entrena, Radiation Testing of a Multiprocessor Macrosynchronized Lockstep Architecture With FreeRTOS, IEEE Trans on Nuclear Science, 69(3), 462-469, 2022. (2/6) AC: A. Lindoso.
5. M. Peña-Fernández, A. Lindoso, L Entrena, I Lopes, V. Pouget., Microprocessor Error Diagnosis by Trace Monitoring Under Laser Testing, IEEE Trans on Nuclear Science, 68(8), 2021. (2/5) AC. A. Lindoso.

6. M. Peña-Fernández, A. Lindoso, L. Entrena, M. Garcia-Valderas., Error Detection and Mitigation of Data-Intensive Microprocessor Applications Using SIMD and Trace Monitoring, IEEE Trans on Nuclear Science, 67(7), 2020. (2/5) AC: A. Lindoso.
7. M. Peña-Fernandez, A. Lindoso, L. Entrena, M. Garcia-Valderas, Y. Morilla, P. Martín-Holgado, Online Error Detection Through Trace Infrastructure in ARM Microprocessors, IEEE Trans on Nuclear Science, 66(7), 2019. (2/6) AC A. Lindoso.
8. A. Lindoso, M. García-Valderas, L. Entrena, Y. Morilla, P. Martín-Holgado, Evaluation of the suitability of NEON SIMD microprocessor extensions under proton irradiation, IEEE Trans on Nuclear Science. 64(1), 2018. (1/5) AC: L. Entrena.
9. A. Lindoso, L. Entrena, M. Garcia-Valderas, L. Parra, A hybrid fault-tolerant LEON3 soft core processor implemented in low-end SRAM FPGA. IEEE Trans on Nuclear Science. 64(1), 2017. (1/4), AC: L. Entrena.
10. L. Parra, A Lindoso, M Portela-Garcia, L. Entrena, B. Du, M. Sonza Reorda, L. Sterpone, A New Hybrid Nonintrusive Error-Detection Technique Using Dual Control-Flow Monitoring, IEEE Trans. on Nuclear Science, 61(6), 2014. (2/7) AC: L. Entrena.

C.2. Congress

1. P. Aviles et al, Acceleration of the TSDCE MIMO Channel Estimation Algorithm on a Multi-core Platform, EATIS '22: Proceedings of the 11th Euro American Conference on Telematics and Information Systems, 2022, Pages 1–4. Poster.
2. P. Aviles, L. Garcia, J. Belloch, L. Entrena, A. Lindoso, Comparative of proton radiation data for 28 nm Zynq-7000 SoC, RADECS 2022 Data Workshop, Venice, Italy. Poster.
3. P. Aviles, J. Belloch, A. Lindoso, L. Entrena, Evaluating Fundamental Matrix Operations on Multi-core System-on-Chip, 2021 Conference on Design of Circuits and Integrated Systems (DCIS), Vila Do Conde, Portugal. Poster.
4. G. León, J. M. Badía, J. A. Belloch, A. Lindoso, L. Entrena, Evaluating the soft-error sensitivity of LU decomposition on low-power and high-end GPUs, 32th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF), 2021, Bordeaux, France. Poster.
5. L. A. García-Astudillo, A. Lindoso, M. Portela and L. Entrena, Evaluation of a Reduced Precision Redundancy FFT Design, 2020 Conference on Design of Circuits and Integrated Systems (DCIS), Segovia, Spain, 2020, pp. 1-6. (IEEEExplore) oral.
6. Y. Morilla et al., Progress of CNA to become the Spanish facility for combined irradiation testing in aerospace, RADECS 2018 18th, Goteborg, Sweden, 2018, pp. 1-5. (IEEEExplore) poster.
7. L. Entrena et al, Flexible Approaches to Fault-Tolerant Microprocessors for Space Applications, DATA Systems in Aerospace, Proceedings of the conference, 2015, Barcelona, Spain. Edited L. Ouwehand. ESA-SP Vol. 732, 2015. Oral.
8. P. Palomo et al, A HW-SW Co-Designed System for the Lunar Lander Hazard Detection and Avoidance Breadboarding, DASIA 2014 - DATA Systems In Aerospace, Proceedings of the conference, 2014, Warsaw, Poland. Edited by L. Ouwehand. ESA SP Vol. 725. ISBN: 978-92-9221-289-6, id.60. Oral.
9. L. Parra, A. Lindoso and L. Entrena, "Comparative of software-based hardening techniques for LEON 3 microprocessor," Design of Circuits and Integrated Systems, Madrid, Spain, 2014. (IEEEExplore) Oral.
10. B. Du et al., "Exploiting the debug interface to support on-line test of control flow errors," 2013 IEEE 19th International On-Line Testing Symposium (IOLTS), Chania, Greece, 2013, pp. 98-103. Oral.

C.3. Research projects,

1. PDC2023-145852-C21, Modulos Hardware de Alta Fiabilidad para RISC-V. IP: L. Entrena & M. García-Valderas. Implementation of fault tolerant solutions for RISC-V architecture with application to aerospace sector.
2. PID2022-138696OB-C21, NeCOT-Enfoques Hardware para la utilización de COTS en New Space. IP: A. Lindoso & M. Garcia Valderas.(137,500€). Study the reliability and adapt the architecture and software of COTS complex digital systems for their use in Space.

3. RADNEXT - RADIation facility Network for the EXploration of effects for indusTry and research, EUROPEAN COMMISSION RESEARCH EXECUTIVE AGENCY 2021 – 2025. Researcher, task: facility comparative for complex systems. CERN leads this project in which all European irradiation facilities participate.
4. PID2019-106455GB-C21, RENASER4 Técnicas de endurecimiento hardware e híbridas para SoCs heterogéneos en aplicaciones. Researcher, tasks: microprocessors and high performance systems reliability.
5. HUBS 2018/MadridFlightOnChip, Consortium Madrid for next generation Flight Systems based on Multiprocessor System On a Chip Technology, EU/CAM, 2019-2022. IP DMA group: A. Lindoso & L. Entrena (243,527.53€). Technological HUB project led by Sener Aeroespacial. Our team tasks: reliable electronic design with COTS.
6. Verification of SEU-mitigation techniques in 3rd/4th generation Flash FPGAs. ESA Contract 4000123942/18/NL/GLC. 07/06/2018-07/12/2019. Researcher, task: design of formal verification tool.
7. ESP2015-68245-C4-1-P, Diseño y verificación de circuitos electrónicos a escala nanométrica para aplicaciones espaciales y terrestres en ambientes de radiación (RENASER3) Ministerio de Economía y Competitividad, 2016-2019. Researcher, task: Fault tolerant microprocessors and FPGAs and fault injection tools.
8. TEC2010-22095-C03-03, Análisis integral de circuitos y sistemas digitales para aplicaciones aeroespaciales. (Renaser+), Ministerio de Ciencia e Innovación. (2011-2014). Researcher, tasks: Digital circuits fault injection tools and soft core microprocessors reliability.
9. IPT-20111022, PERIGEO-Plataformas Aéreas de Investigación y Ensayos Orbitales.CDTI.INNPRONTA 2011-2015. Researcher, tasks: image processing algorithms hardware acceleration, adaptation of UAV image processing algorithms for approximation and landing in celestial bodies

C.4. Contracts, technological or transfer merits

1. Contracts with Sener Aeroespacial and Indra for the project LINCE (Tecnologías avanzadas para líneas de producción en serie de cargas de pago y plataformas espaciales, PTEG-20241001), led by Indra, (12,74M€).
2. Research of large 2D FFT implementation on FPGA, Deimos Space, S.L., 2023. Researcher: Hardware designer.
3. Industrial PhD 2022 with Arquimea, the research results were selected for ESA funding in a competitive call in OSIP channel (OSIP Idea: I-2020-02664), ESA contract: 4000136081: "Online detection and diagnosis for radiation-induced errors in COTS microprocessors" (175,000€). (2021-2023), UC3M IP: A. Lindoso (PC/22/03/00096), (40,000€), Arquimea Technical Project Manager: Manuel Peña (Industrial PhD funded by CAM).
4. Sistema de provisión y consumo de contenidos multimedia HD en medios de transporte colectivo de viajeros basado en la tecnología LiFi para la transmisión de datos, Optiva Media, 2019-2022. Researcher: sw control, integration and test of embedded system.
5. Diseño e integración (SW) para una FPGA de la capa física del estándar LiFi, Universidad Complutense (2017). Researcher: sw control, integration and test of embeded system.
6. Radiation Hardening of a Polyphase-FFT Demultiplexer. THALES ALENIA SPACE FRANCE, 01/12/2014- 15/04/2015. IP: A. Lindoso & M. Portela (30,000€). Design and hardening of a polyphase filter (oriented to satellite applications). In the project was used AMUSE tool (DMA fault injector) to detect the less reliable parts of the circuit.
7. Front-end readout ASIC technology study and development test vehicles for front-end readout ASICS - ASIC SEDUCE MF, Arquimea, 2010-2016.